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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,132	03/01/2002	Tomohiro Morimura	50006-140	5653

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EXAMINER	
REILLY, SEAN M	

ART UNIT	PAPER NUMBER
2153	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/085,132	MORIMURA ET AL.	
	Examiner	Art Unit	
	Sean Reilly	2153	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5,7 and 9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7 and 9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/13/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to Applicant's amendment and request for reconsideration filed on February 13, 2006. Claims 1, 3, 5, 7, and 9 are presented for further examination.

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on February 13, 2006 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Specification

2. The new title submitted by Applicant on February 13, 2006 is accepted and entered into the record.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3, 5, 7, and 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwai et al. (Architecture of Compiler-Initiative Type Multiprocessor ASCA, English translation cited in the attached 892; hereinafter Iwai).

4. With regard to claim 1, Iwai disclosed a multi-processor system apparatus having a plurality of processors connected to each other by a network arrangement, comprising:

- a multiplicity of processor elements, each processor element including a processor, a memory, and an interface for connection with said network arrangement (Section 3.1); and
- an array of multi-stage interconnection networks having a multiple stage connection arrangement where multiple stages of switching elements are provided for interconnection between said processor elements (Section 3.1), wherein said processor elements and said multi-stage interconnection networks are grouped to clusters based on a specific number and arranged in multiple levels (R-Clos 2000, pg 14 – Section 5) and the transfer of data packets between said processor elements is conducted according to a schedule statically determined with the use of switching state tables which are generated at different timings and indicate the status of the switching elements in said multi-stage interconnection networks (Section 5.2).
- said multi-stage interconnection networks of a multiple stage connection arrangement are classified into two functions, an upstream linking network for upward transfer of data packets from the lower stage to the upper stage and a downstream linking network for downward transfer of data packets from the upper stage to the lower stage (See inter alia sections 3.1 and 5, where Iwai supports the flow of packets between processors in both directions of the multi-stage network bus or in other words supports both the upstream and downstream flow of data packets).

5. With regard to claim 3, Iwai disclosed said switching status table comprises data of a packet assigned to a particular output port, data of other packets demanding the connection to the output port, and data of the status of the output port of each switching element (Parallel processing sections pg 6 and Section 5.2).

6. With regard to claim 5, Iwai disclosed when the connection to the output port of any switching element is demanded by two or more packets at the same timing, the transfer of packets between said processor elements is conducted as scheduled across said multi-stage interconnection networks so that a packet not assigned to the output port through a specific manner of arbitration is permitted to demand the output port with a switching status table at another timing (Scheduling - Section 5.2, also refer to parallel processing granularity – section 3.2).

7. With regard to claim 7, Iwai disclosed said multi-stage interconnection networks are of a cross connection arrangement and when the connection to the output port of any switching element is demanded by two or more packets at the same timing, the transfer of packets between said processor elements is conducted as scheduled across said multi-stage interconnection networks so that a packet not assigned to the output port through a specific manner of arbitration is permitted to demand another output port which is not demanded by other packets (Scheduling - Section 5.2, also refer to parallel processing granularity – section 3.2).

8. With regard to claim 9, Iwai disclosed the scheduling for each packet is preliminarily conducted by a compiler (Compiler Section 5.2).

Response to Arguments

9. In response to Applicant's request for reconsideration filed on February 13, 2006, the following factual arguments are noted:

a. Iwai failed to disclose multi-stage interconnection network of a multiple stage connection arrangement are classified into two functions, an upstream linking network for upward transfer of data packets from the lower stage to the upper stage and a downstream linking network for downward transfer of data packets from the upper stage to the lower stage.

In considering (a), Examiner respectfully disagrees with Applicant's argument. Iwai clearly disclosed classifying the multistage interconnection networks of a multiple stage connection into two **functions**, an upstream linking network for upward transfer of data packets from the lower stage to the upper stage and a downstream linking network for downward transfer of data packets from the upper stage to the lower stage. See for instance inter alia sections 3.1 and 5, where Iwai supports the flow of packets between processors in both directions of the multi-stage network bus or in other words supports both the upstream and downstream flow of data packets. Note based on Applicant's arguments it appears that Applicant intends to further limit the claims to a dedicated upstream path and a dedicated downstream path for the flow of packets. The current claims are certainly not that limiting and merely call for classifying the multistage interconnection networks of a multiple stage connection into **two functions** (and not dedicated network paths).

Conclusion

10. The prior art made of record, in PTO-892 form, and not relied upon is considered pertinent to applicant's disclosure.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sean Reilly whose telephone number is 571-272-4228. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Glen Burgess can be reached on 571-272-3949. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

May 2, 2006

KRISNA LIM
PRIMARY EXAMINER